

Fig. 1 PRIOR ART

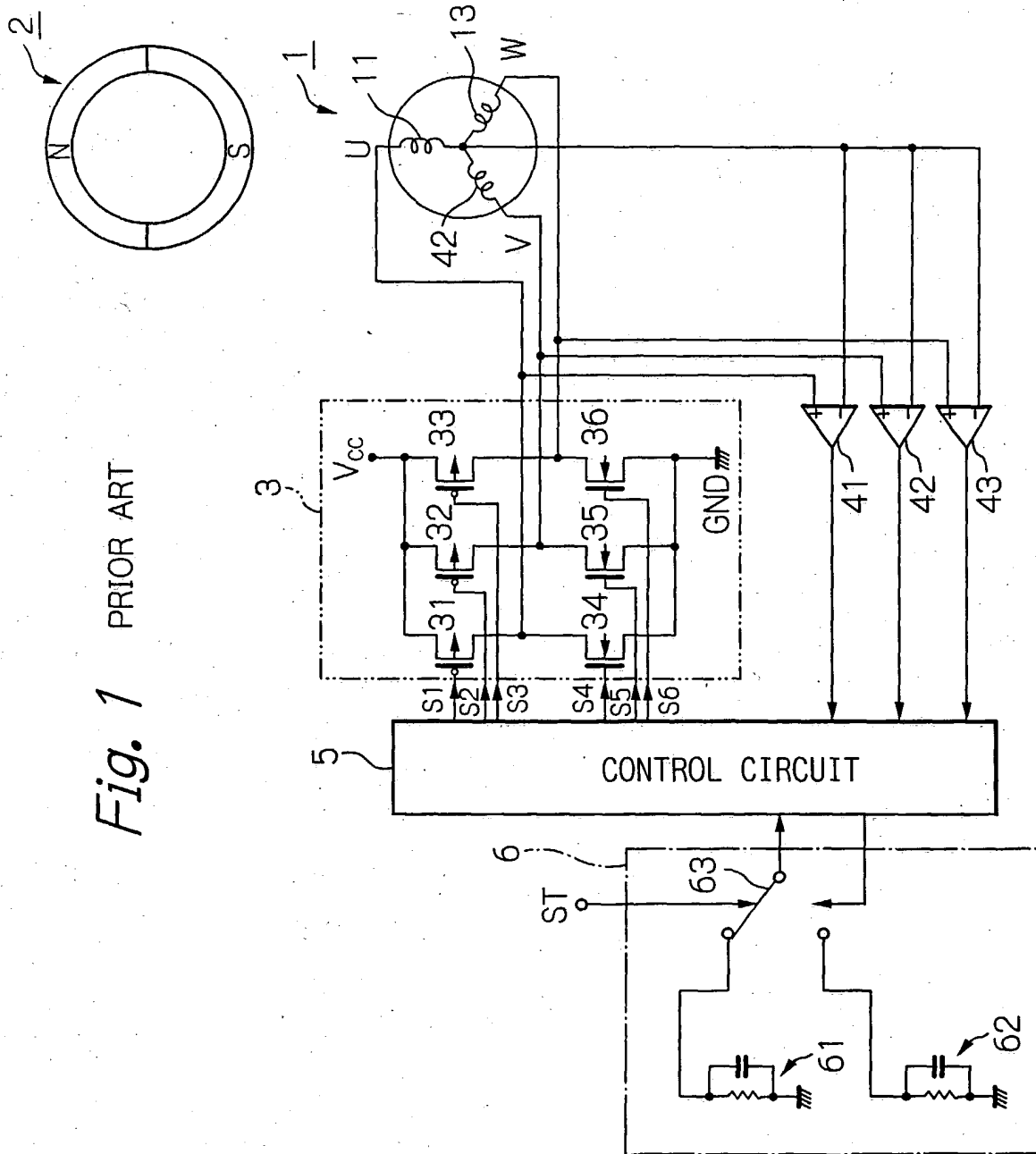


Fig. 2 PRIOR ART

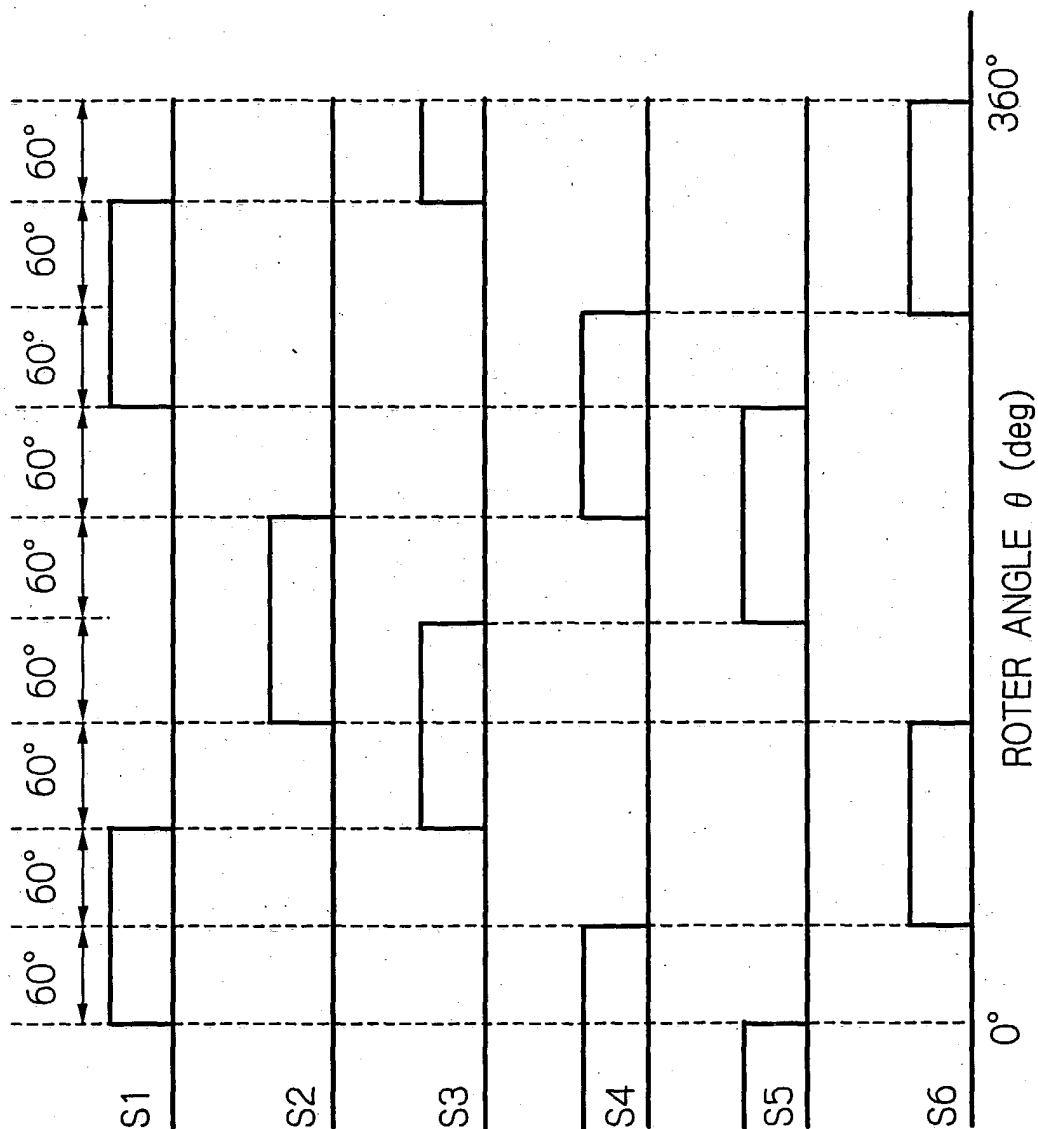


Fig. 3

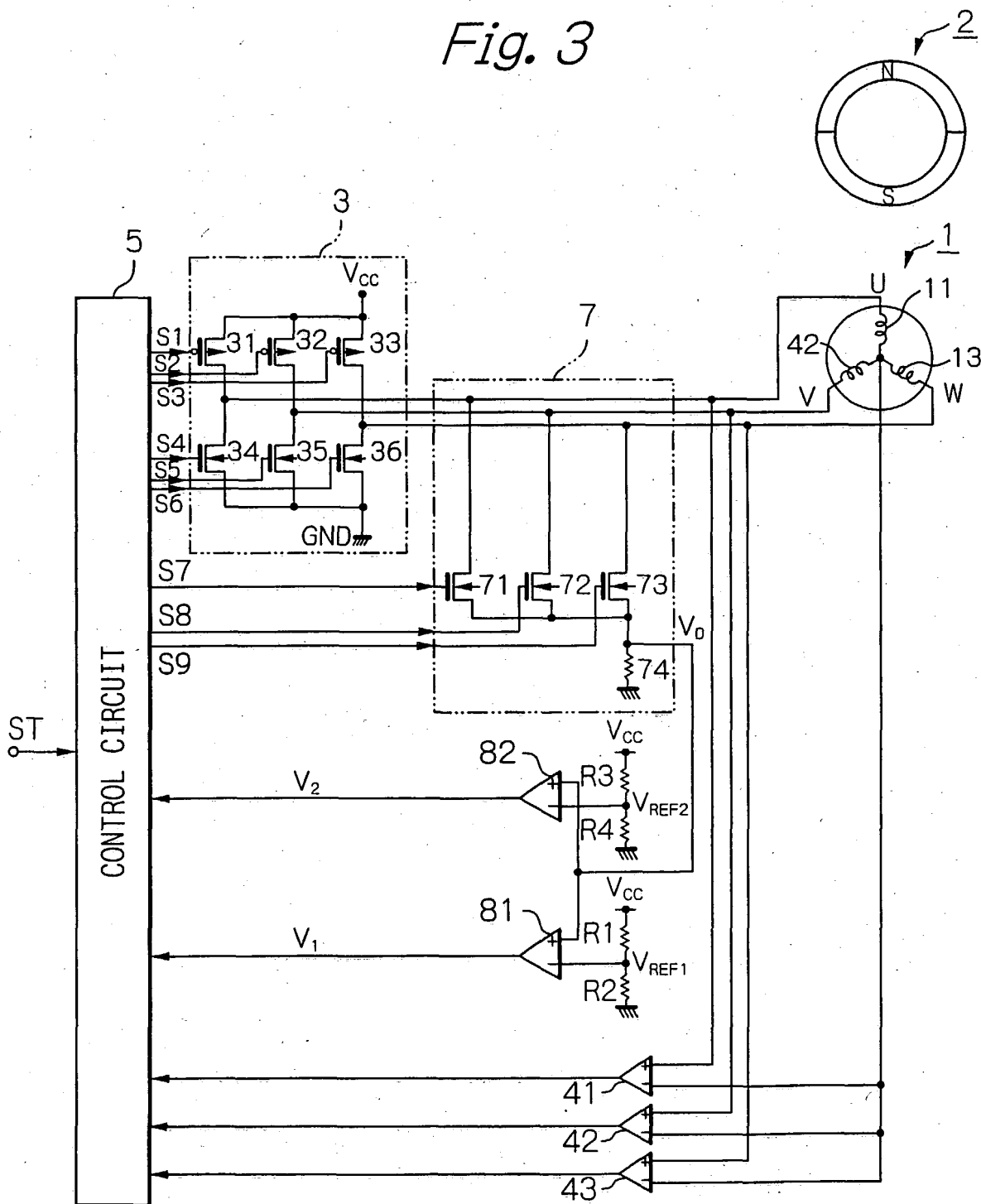


Fig. 4

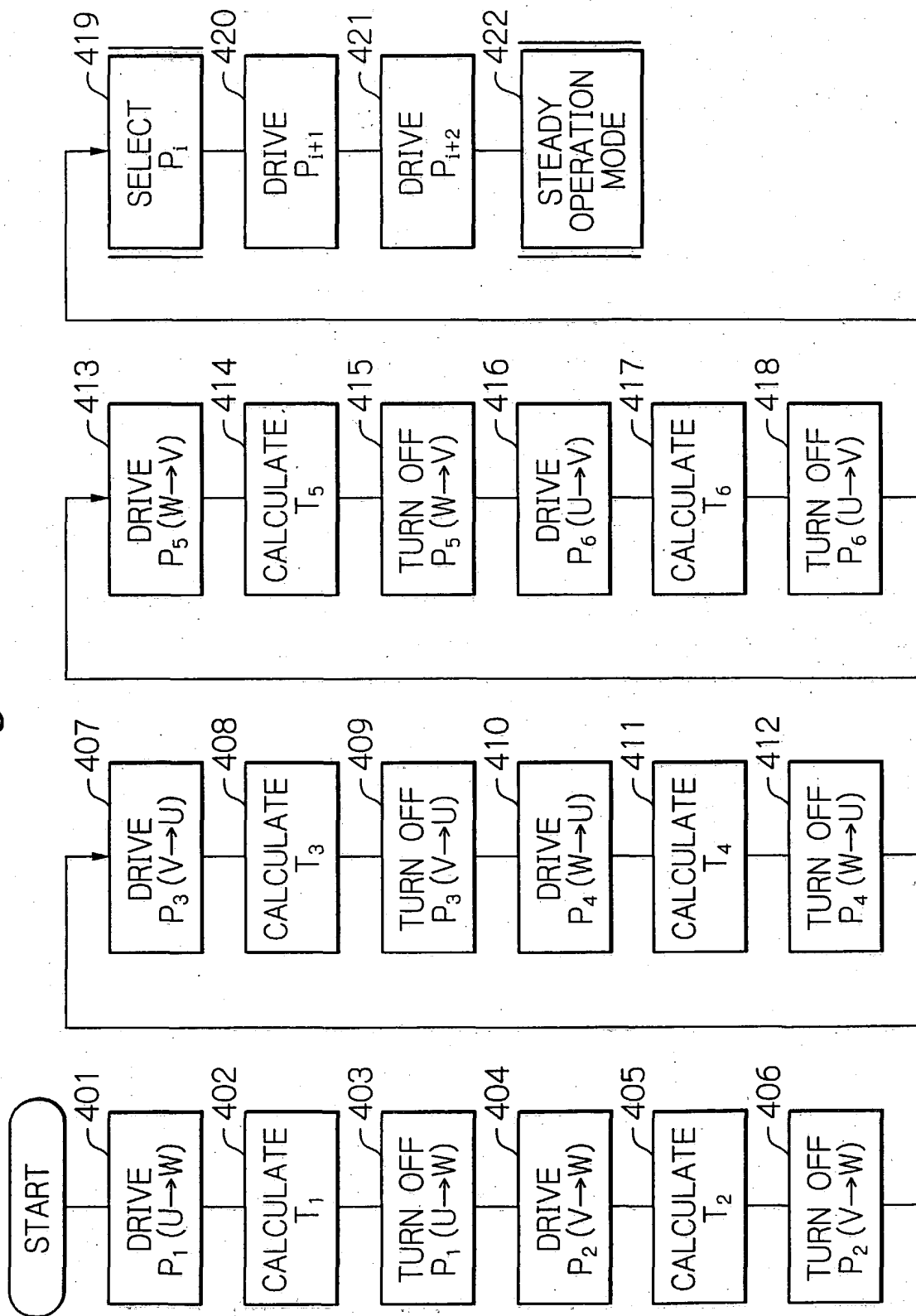


Fig. 5

DRIVER PHASE	CURRENT
P ₁	U → W
P ₂	V → W
P ₃	V → U
P ₄	W → U
P ₅	W → V
P ₆	U → V

Fig. 6

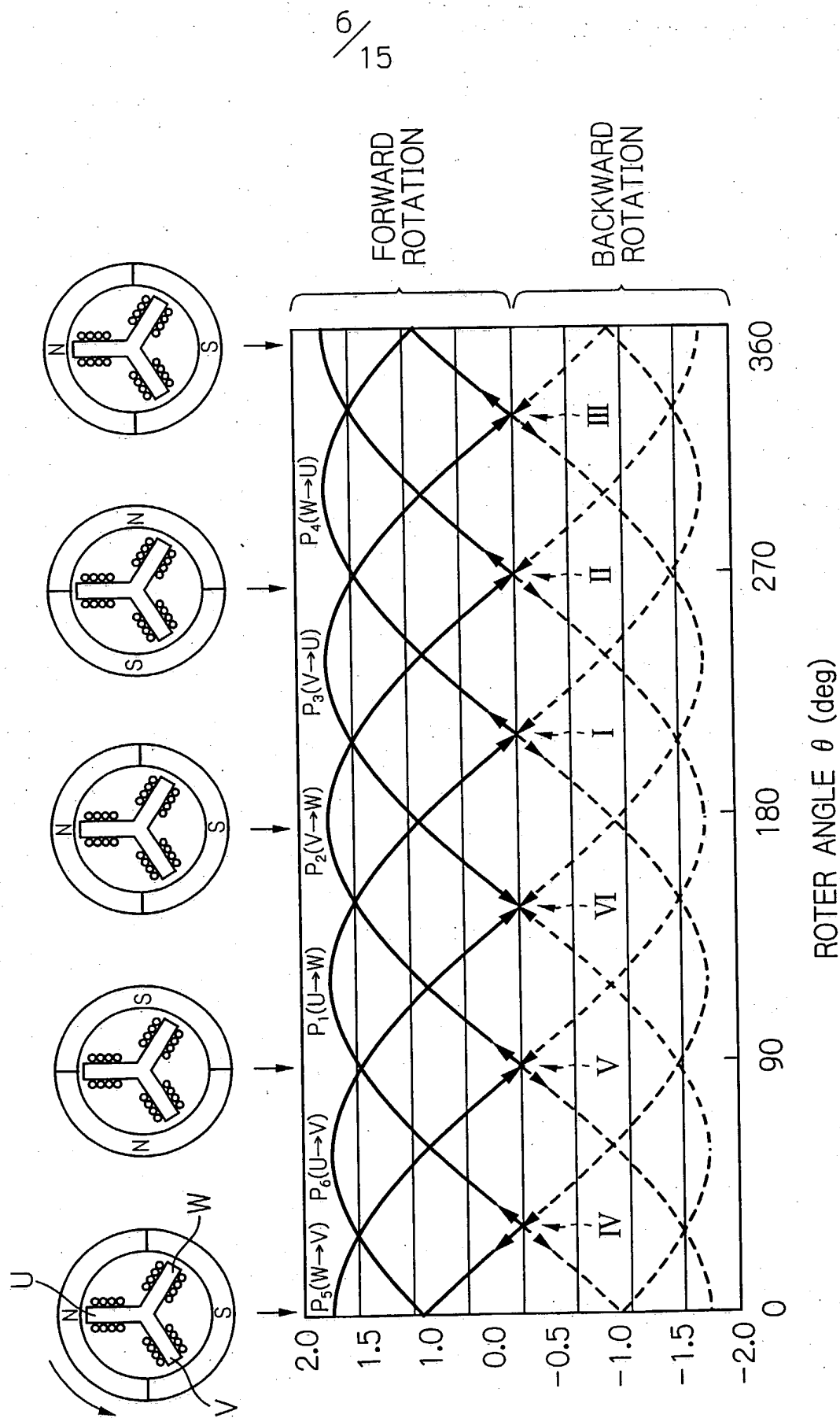


Fig. 7

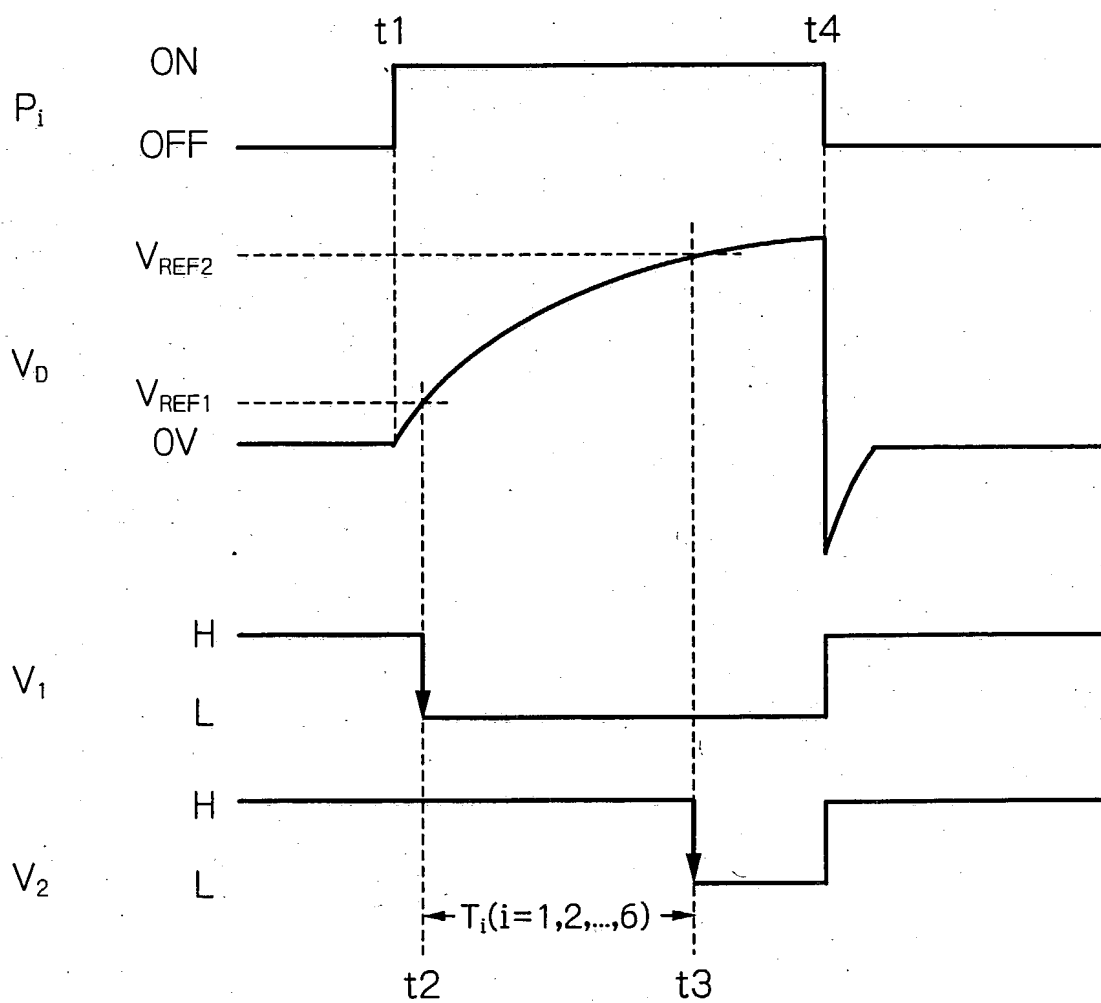
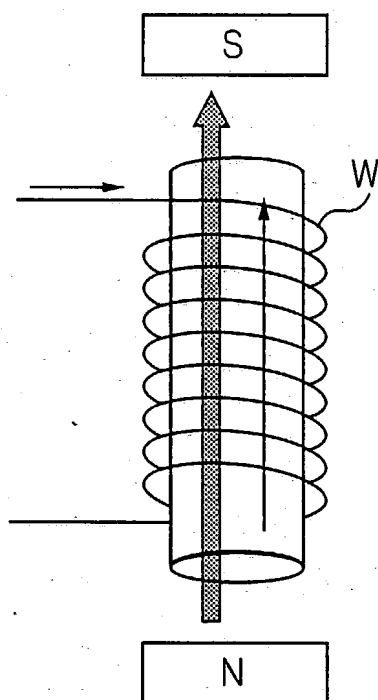
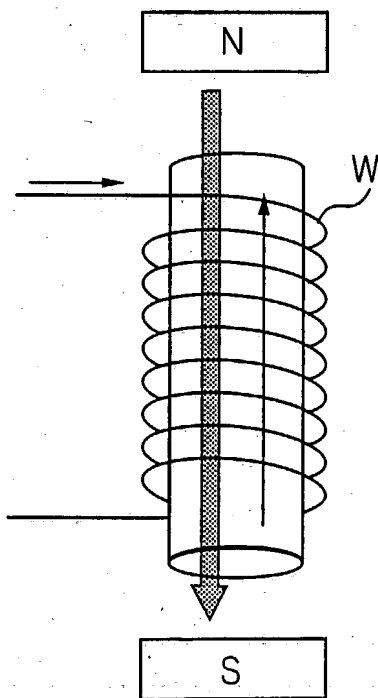


Fig. 8A

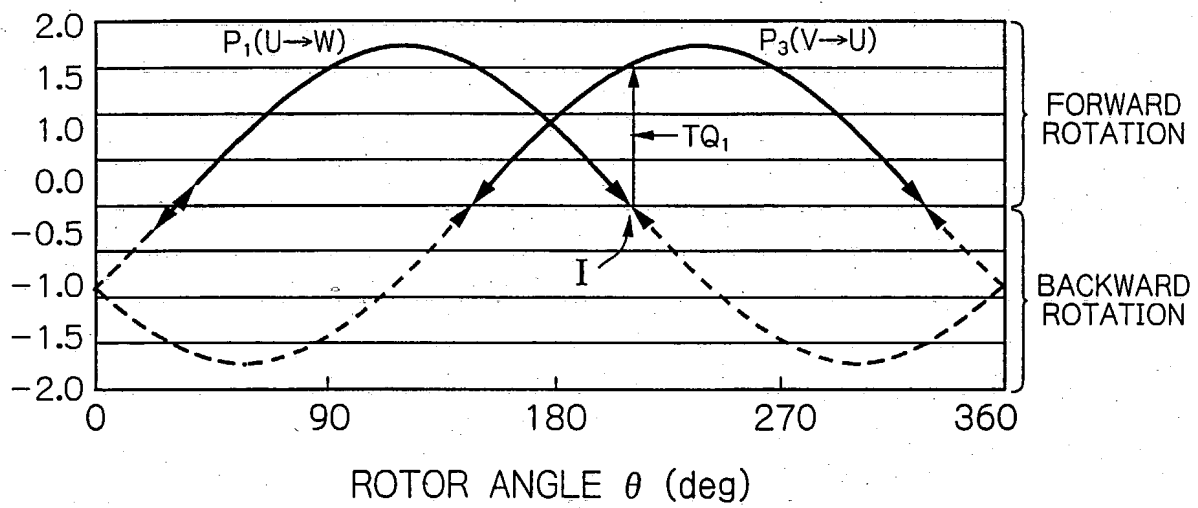


L : MINIMUM

Fig. 8B



L : MAXIMUM

Fig. 9

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Fig. 10A

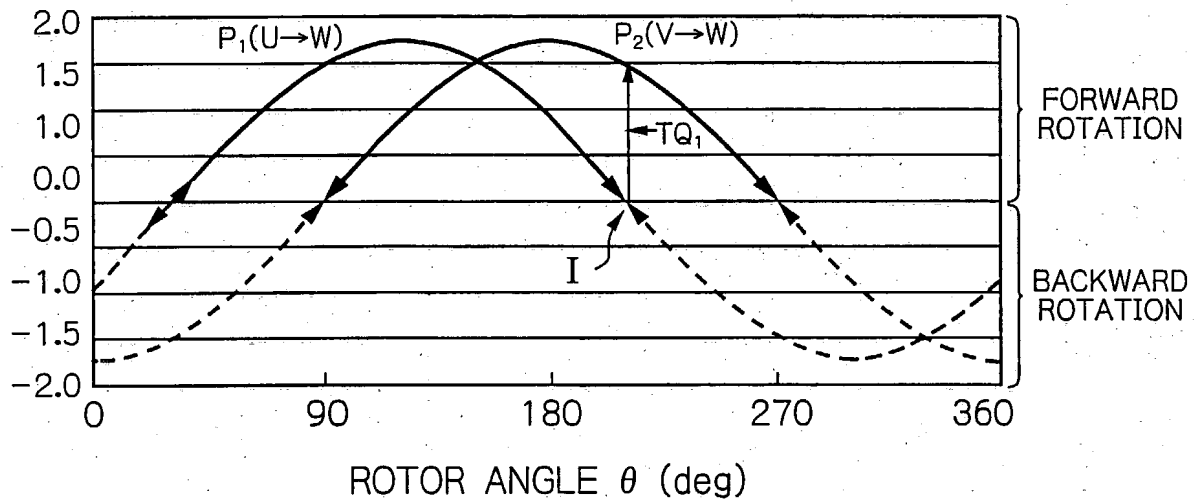


Fig. 10B

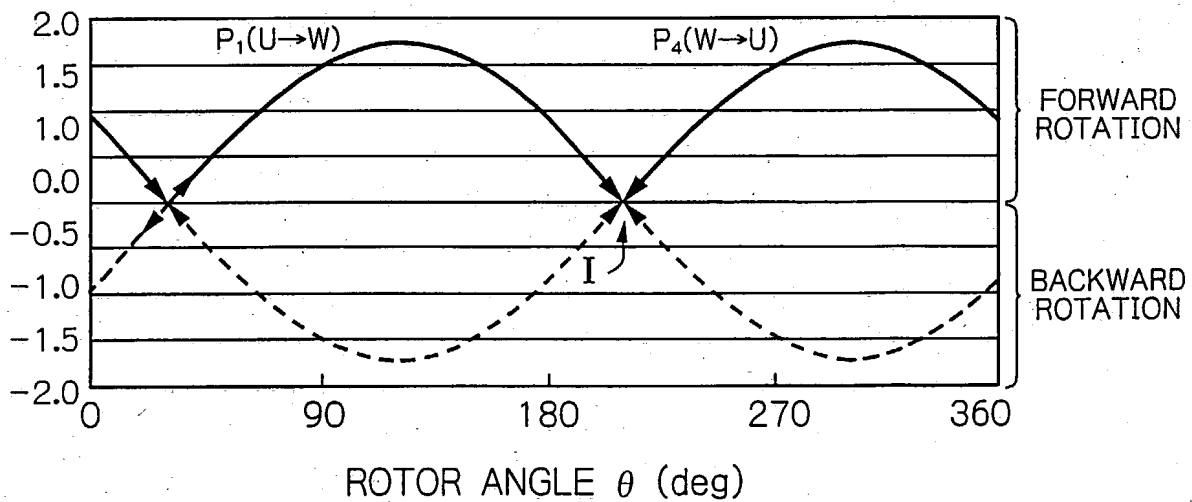
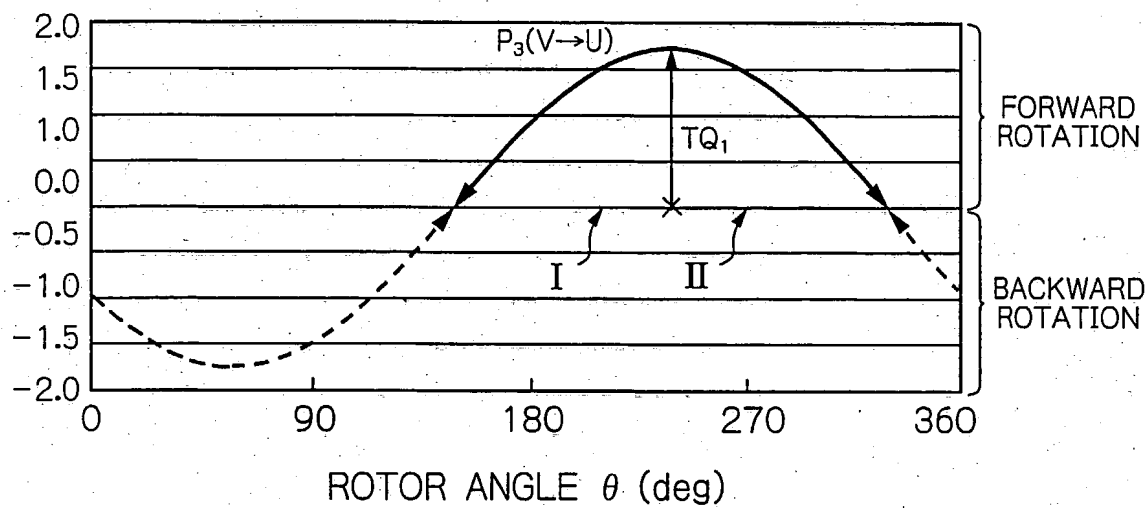
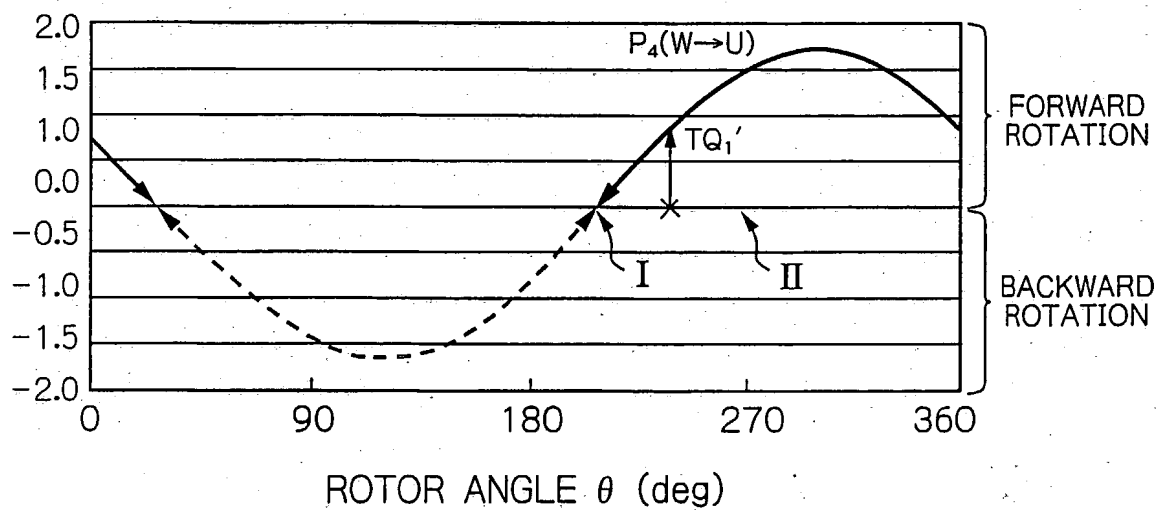


Fig. 11A



θ

Fig. 11B



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Fig. 12

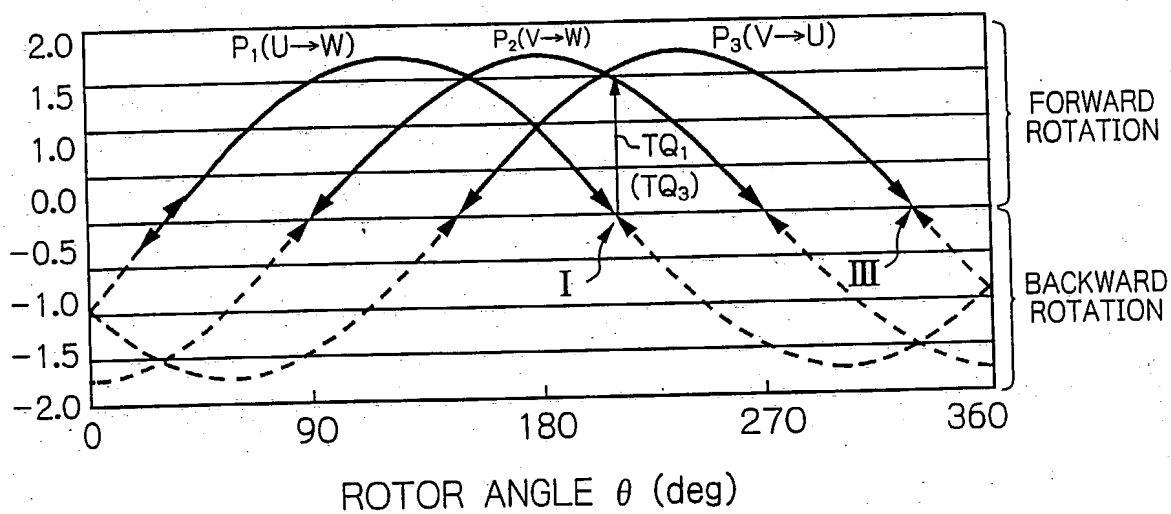


Fig. 13A

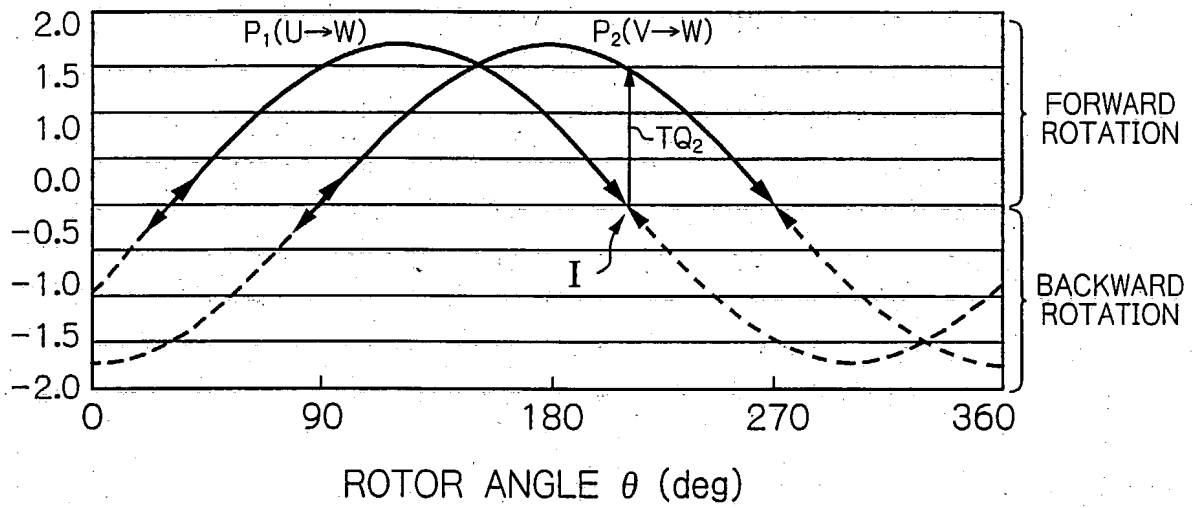


Fig. 13B

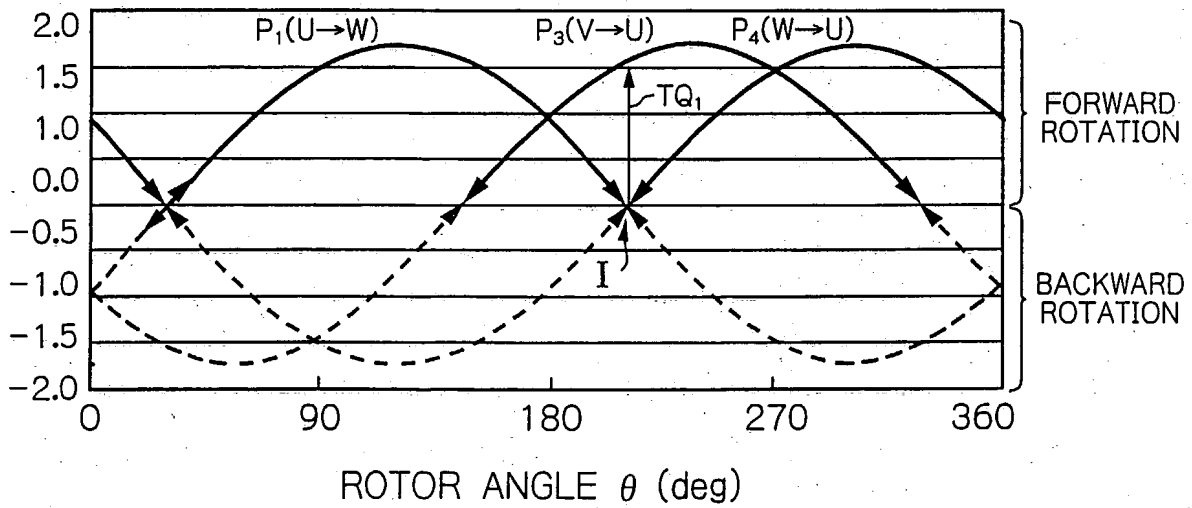


Fig. 14A

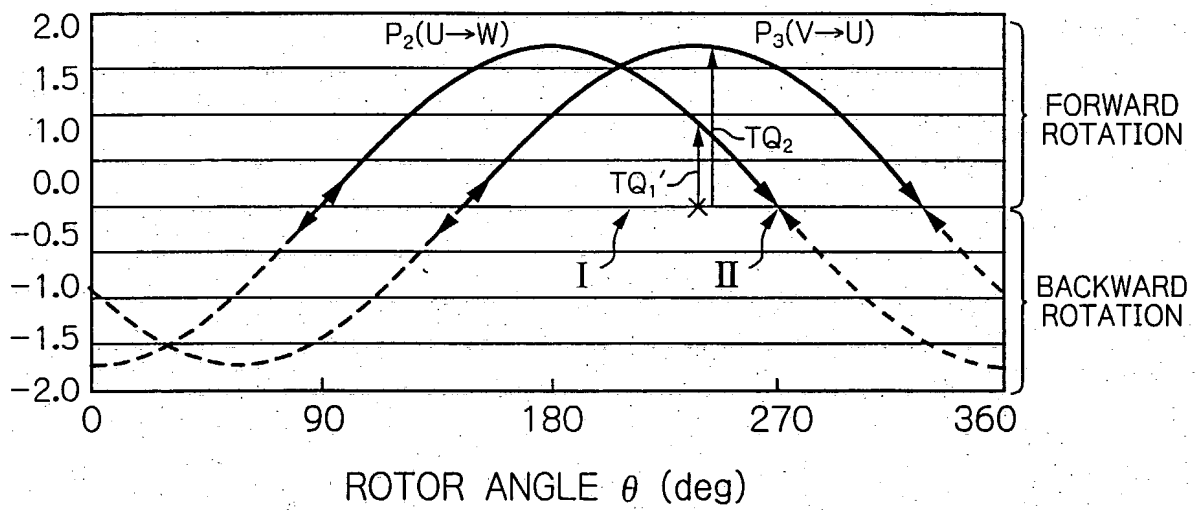


Fig. 14B

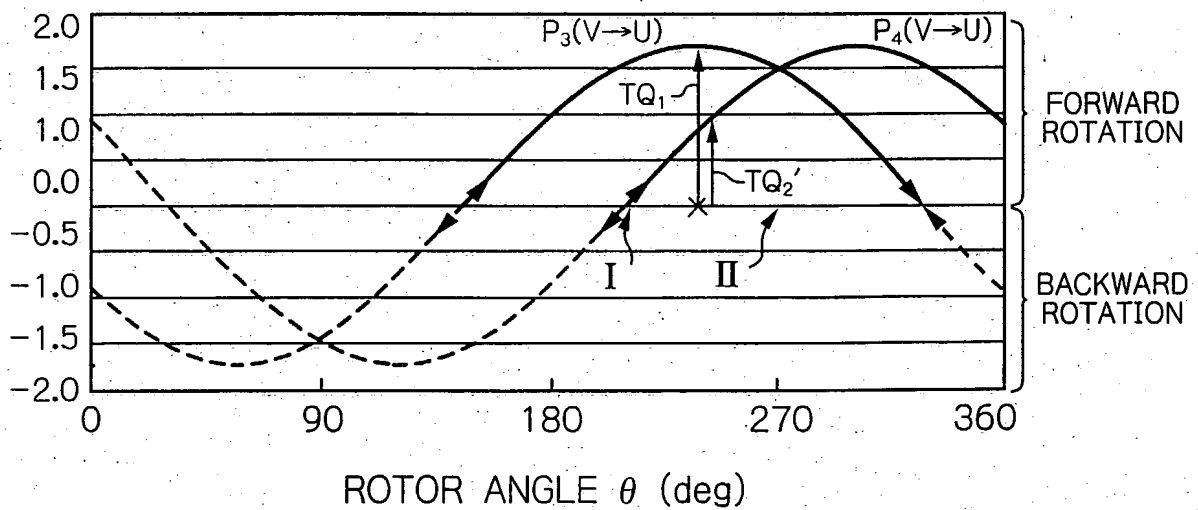


Fig. 15

